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AMENDMENTS TO THE CLAIMS

Please amend the claims as follows:

1. (currently amended) A method of making ~~an~~ a plurality of electrically programmable memory elements, comprising:

providing a first dielectric layer, said first dielectric layer having an opening, said opening having ~~a~~ first and second sidewall surfaces and a bottom surface;

forming a conductive layer on said sidewall surfaces and on ~~a portion of~~ said bottom surface of said opening~~, said portion being less than the entire bottom surface~~;

removing at least a portion of said conductive layer from said bottom surface, thereby electrically isolating portions of said conductive layer formed on said first and second sidewalls, one from the other;

forming a second dielectric layer ~~on said conductive layer, said second dielectric layer~~ contacting said bottom surface of said opening; and

forming a programmable resistance material in electrical communication with top portions of said electrically isolated portions of said conductive layer.

Claims 2-6. (canceled)

7. (previously presented) The method of claim 1, wherein said programmable resistance material is a phase-change material.

8. (original) The method of claim 1, wherein said programmable resistance material includes a

chalcogen element.

9. (original) The method of claim 1, wherein said first dielectric layer and said second dielectric layer are formed of the same material.

Claims 10-15. (canceled)

16. (previously presented) The method of claim 1, wherein said forming a conductive layer comprises conformally depositing said conductive layer.

17. (previously presented) The method of claim 1, wherein said forming a conductive layer comprises anisotropically etching said conductive layer.

18. (previously presented) The method of claim 1, wherein said programmable resistance material is electrically coupled to a top surface of said conductive layer.

19. (previously presented) The method of claim 1, wherein said conductive layer includes a conductive sidewall spacer.

20. (currently amended) A method of making ~~an~~ electrically programmable memory elements, comprising:

providing a first and second sidewall surfaces and an adjoining bottom surface;

forming a conductive layer on said sidewall surfaces and on a portion of said bottom surface, said portion being less than the entire bottom surface and thereby electrically isolating the conductive layer on the first sidewall surface from the conductive layer on the second sidewall surface;

forming a dielectric material ~~on said conductive layer, said dielectric material~~ contacting said bottom surface of said opening; and

forming a programmable resistance material in electrical communication with said conductive layer.

21. (previously presented) The method of claim 20, wherein said forming a conductive layer comprises conformally depositing said conductive layer.

22. (previously presented) The method of claim 20, wherein said forming a conductive layer comprises anisotropically etching said conductive layer.

23. (previously presented) The method of claim 20, wherein said programmable resistance material is electrically coupled to a top surface of said conductive layer.

Claim 24. (Canceled)

25. (previously presented) The method of claim 20, wherein said dielectric material is formed on said conductive layer before said forming a programmable resistance material.

26. (previously presented) The method of claim 20, wherein said sidewall surface is the sidewall surface of a dielectric layer.

Claims 27 and 28. (canceled)

29. (previously presented) The method of claim 26, wherein said dielectric material and said dielectric layer are formed of the same material.

30. (currently amended) A method of making an electrical device, comprising:

providing a first and second sidewall surfaces and an adjoining bottom surface;

forming a conductive layer on said sidewall surfaces and on a portion of said bottom surface, said portion being less than the entire bottom surface and thereby electrically isolating the conductive layer on the first sidewall surface from the conductive layer on the second sidewall surface;

forming a dielectric material ~~on said conductive layer, said dielectric material~~ contacting said bottom surface of said opening; and

forming a chalcogenide material in electrical communication with said conductive layer.

31. (previously presented) The method of claim 30, wherein said forming a conductive layer comprises conformally depositing said conductive layer.

32. (previously presented) The method of claim 30, wherein said forming a conductive layer comprises anisotropically etching said conductive layer.

33. (previously presented) The method of claim 30, wherein said chalcogenide material is electrically coupled to a top surface of said conductive layer.

Claim 34. (canceled)

35. (previously presented) The method of claim 30, wherein said dielectric material is formed before said forming a chalcogenide material.

36. (previously presented) The method of claim 30, wherein said sidewall surface is the sidewall surface of a dielectric layer.

Claims 37 and 38. (canceled)

39. (previously presented) The method of claim 36, wherein said dielectric material and said dielectric layer are formed of the same material.

40. (previously presented) The method of claim 30, wherein said conductive layer includes a conductive sidewall spacer.

41. (currently amended) A method of making an electrical device, comprising:

forming ~~an~~ electrical contacts by a method comprising:

providing a first and second sidewall surfaces and an adjoining bottom surface;

forming a conductive layer on said sidewall surfaces and on a portion of said bottom surface, said portion being less than the entire bottom surface and thereby electrically isolating the conductive layer on the first sidewall surface from the conductive layer on the second sidewall surface;

forming a dielectric material ~~on said conductive layer, said dielectric material~~ contacting said bottom surface of said opening; and

forming a chalcogenide material in electrical communication with said electrical contact.

42. (previously presented) The method of claim 41, wherein said forming a conductive layer comprises conformally depositing said conductive layer.

43. (previously presented) The method of claim 41, wherein said forming a conductive layer comprises anisotropically etching said conductive layer.

44. (previously presented) The method of claim 41, wherein said chalcogenide material is formed after forming said electrical contact.

45. (previously presented) The method of claim 41, wherein said electrical contact is a conductive sidewall spacer.

46. (previously presented) The method of claim 41, wherein said sidewall surface is the sidewall surface of a dielectric layer.

47. (currently amended) A method of making an electrical device, comprising:

forming ~~an~~ electrical contacts by a method comprising:

providing a first and second sidewall surfaces and an adjoining bottom surface;

forming a conductive layer on said sidewall surfaces and on a portion of said bottom surface, said portion being less than the entire bottom surface and thereby electrically isolating the conductive layer on the first sidewall surface from the conductive layer on the second sidewall surface;

forming a dielectric material ~~on said conductive layer, said dielectric material~~ contacting said bottom surface of said opening; and

forming a phase-change material, in electrical communication with said electrical contact.

48. (previously presented) The method of claim 47, wherein said forming a conductive layer comprises conformally depositing said conductive layer.

49. (previously presented) The method of claim 47, wherein said forming a conductive layer comprises anisotropically etching said conductive layer.

50. (previously presented) The method of claim 47, wherein said phase-change material is formed after forming said electrical contact.

51. (previously presented) The method of claim 47, wherein said electrical contact is a conductive sidewall spacer.

52. (previously presented) The method of claim 47, wherein said sidewall surface is the sidewall surface of a dielectric layer.

53. (previously presented) The method of claim 47, wherein said phase-change material comprises at least one chalcogen element.

Claims 54-57. (canceled)

58. (previously presented) The method of claim 18, wherein said top surface of said conductive layer has a lateral dimension less than 1000 Angstroms.

59. (previously presented) The method of claim 20, wherein said portion of the bottom surface is a surface of a substrate.

60. (previously presented) The method of claim 20, wherein said conductive layer has an area of contact with said programmable resistance material, the area of contact having a dimension less than 1000 Angstroms.

61. (previously presented) The method of claim 20, wherein said forming a conductive layer comprises forming a dual-layered conductive sidewall spacer.

62. (previously presented) The method of claim 61, wherein said dual-layered conductive sidewall spacer comprises a first layer having a first resistivity and a second layer having a second resistivity, said first resistivity being less than said second resistivity.

63. (previously presented) The method of claim 30, wherein a top surface of said conductive layer is in electrical communication with said chalcogenide material.

64. (previously presented) The method of claim 63, wherein said top surface has an area of contact with said chalcogenide material, the area of contact having a dimension less than 1000 Angstroms.

65. (previously presented) The method of claim 30, wherein said portion of the bottom surface is a surface of a substrate.

66. (previously presented) The method of claim 40, wherein said conductive sidewall spacer is a dual-layered conductive sidewall spacer.

67. (previously presented) The method of claim 66, wherein said dual-layered conductive sidewall spacer comprises a first layer having a first resistivity and a second layer having a second resistivity, said first resistivity being less than said second resistivity.

68. (previously presented) The method of claim 41, wherein said portion of the bottom surface is a surface of a substrate.

69. (previously presented) The method of claim 41, wherein said conductive layer has an area of contact with said chalcogenide material, the area of contact having a dimension less than 1000 Angstroms.

70. (previously presented) The method of claim 41, wherein said forming a conductive layer comprises forming a dual-layered conductive sidewall spacer.

71. (previously presented) The method of claim 70, wherein said dual-layered conductive sidewall spacer comprises a first layer having a first resistivity and a second layer having a second resistivity, said first resistivity being less than said second resistivity.

72. (previously presented) The method of claim 47, wherein said conductive layer has an area of contact with said phase-change material, the area of contact having a dimension less than 1000 Angstroms.

73. (previously presented) The method of claim 47, wherein said portion of the bottom surface is a surface of a substrate.

74. (previously presented) The method of claim 47, wherein said forming a conductive layer comprises forming a dual-layered conductive sidewall spacer.

75. (previously presented) The method of claim 74, wherein said dual-layered conductive sidewall spacer comprises a first layer having a first resistivity and a second layer having a second resistivity, said first resistivity being less than said second resistivity.

Claims 76-87 cancelled

88. (previously presented) The method of claim 1, wherein said conductive layer contacts said bottom surface of said opening.

89. (previously presented) The method of claim 20, wherein said conductive layer contacts said bottom surface of said opening.

90. (previously presented) The method of claim 30, wherein said conductive layer contacts said bottom surface of said opening.

91. (previously presented) The method of claim 41, wherein said conductive layer contacts said bottom surface of said opening.

92. (previously presented) The method of claim 47, wherein said conductive layer contacts said bottom surface of said opening.

93. (previously presented) The method of claim 1, wherein said second dielectric layer fills said opening.

94. (previously presented) The method of claim 20, wherein said dielectric material fills said opening.

95. (previously presented) The method of claim 30, wherein said dielectric material fills said opening.

96. (previously presented) The method of claim 41, wherein said dielectric material fills said opening.

97. (previously presented) The method of claim 47, wherein said dielectric material fills said opening.